JCF60R180S

Product Proposal

600V 180mΩ Superjunction MOSFET

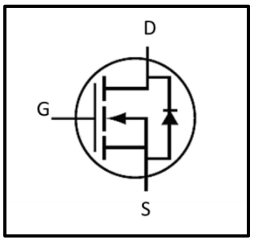
Features

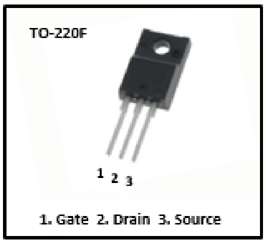
- Advanced superjunction technology
- Ultra-low on-resistance and gate-charge
- RoHS compliant
- 100% avalanche tested

Product Summary	
V_{DS}	600 V
$R_{DS(ON)}$	150 mΩ (Typ.)
	180 mΩ (Max.)
I_D	19 A

Applications

- Server/PC
- Telecom
- LED Applications





Ordering Information

Part Number	Marking	Package	Packaging
JCF60R180S	CF60R180S	TO-220F	Tube

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Drain-to-Source Voltage	V_{DSS}	600	V
Gate-to-Source Voltage	V_{GSS}	±30	V
Continuous Drain Current, Silicon Limited (T_C = 25°C) [1],[2]	I_D	19	A
Continuous Drain Current, Silicon Limited (T_C = 100°C) [1],[2]	I_D	12	A
Pulsed Drain Current [3]	I_{DM}	57	A
Avalanche Energy, Single Pulse [4]	E_{AS}	76	mJ
Power Dissipation (T_C = 25°C)	P_D	36	W
Avalanche Current [4]	I_{AS}	4	A
Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	

Thermal Characteristics

Parameter	Symbol	Max	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	62.5	°C/W
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	3.5	

Static Electrical Characteristics [5]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA	600	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS} , I_D = 1.7 mA	2.5	-	4.5	
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	-	-	1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +30 V	-	-	100	nA
		V_{DS} = 0 V, V_{GS} = -30 V	-	-	-100	nA
Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 8.5 A	-	150	180	mΩ
Gate Resistance	R_G	f = 1 MHz, open drain	-	1.3	-	Ω

Dynamic Electrical Characteristics (5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total Gate Charge	Q_g	V_{GS} = 10 V, V_{DS} = 400 V, I_D = 8.5 A	-	31	-	nC
Gate-to-Source Charge	Q_{gs}		-	6	-	
Gate-to-Drain Charge	Q_{gd}		-	16	-	
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 400 V, I_D = 8.5 A, R_G = 10 Ω	-	12	-	ns
Rise Time	t_r		-	8	-	
Turn-Off Delay Time	$t_{d(off)}$		-	53	-	
Fall Time	t_f		-	10	-	
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 250 kHz, V_{DS} = 400 V	-	1240	-	pF
Output Capacitance	C_{oss}		-	34	-	
Reverse Transfer Capacitance	C_{rss}			3		
Effective Output Capacitance, Energy Related (6)	$C_{o(er)}$	V_{GS} = 0 V, V_{DS} = 0 V to 400 V		54		pF
Effective Output Capacitance, Time Related (7)	$C_{o(tr)}$	V_{GS} = 0 V, V_{DS} = 0 V to 400 V		381		pF

Source Drain Characteristics (5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_F = 8.5 A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	V_R = 400 V, I_F = 8.5 A, dI_F/dt = 100 A/us	-	274	-	ns
Reverse Recovery Charge	Q_{rr}		-	4	-	μC
Peak Reverse Recovery Current	I_{rrm}		-	-	-	A

(1) Limited by maximum $T_{J\,max}$. Maximum duty cycle D=0.75.

(2) Rated according to $R_{\theta JA}$.

(3) Repetitive rating: pulse-width limited by maximum junction temperature.

(4) T_A = 25°C, R_G = 25Ω, I_{AS} = 4 A.

(5) T_J = 25°C unless otherwise specified.

(6) $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is changing from 0 to 400 V.

(7) $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is changing from 0 to 400 V.

Electrical Characteristics Diagrams

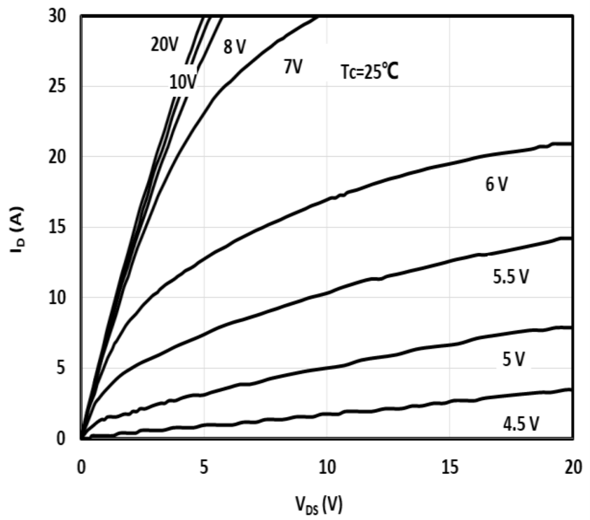


Fig. 1 Typical output characteristics

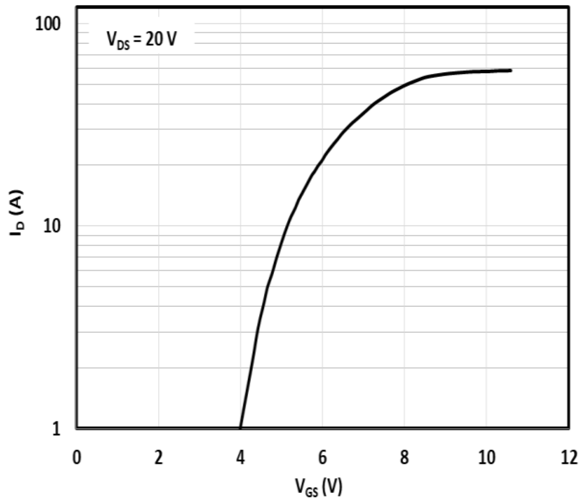


Fig. 2 Typical transfer characteristics

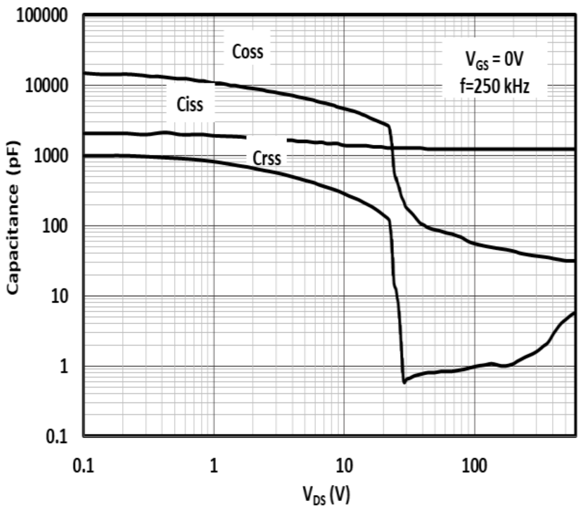


Fig. 3 Typical capacitance characteristics

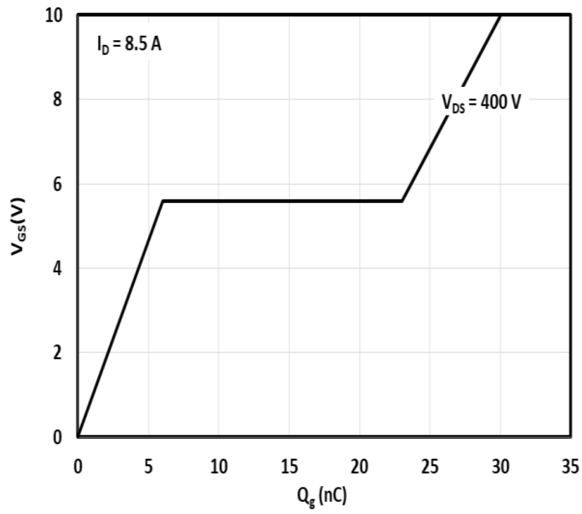


Fig. 4 Typical gate charge characteristics

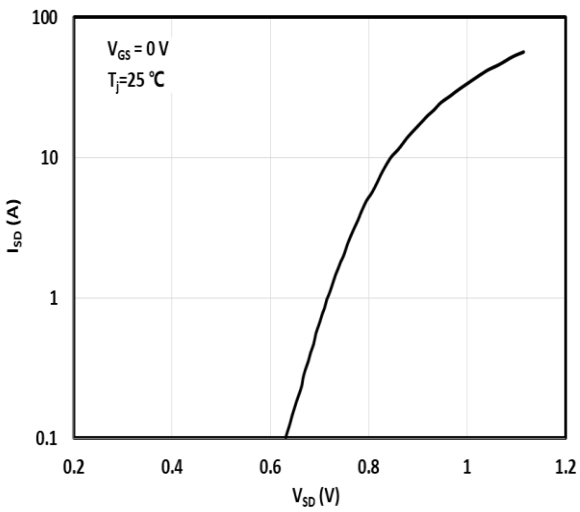


Fig. 5 Typical forward characteristics of body diode

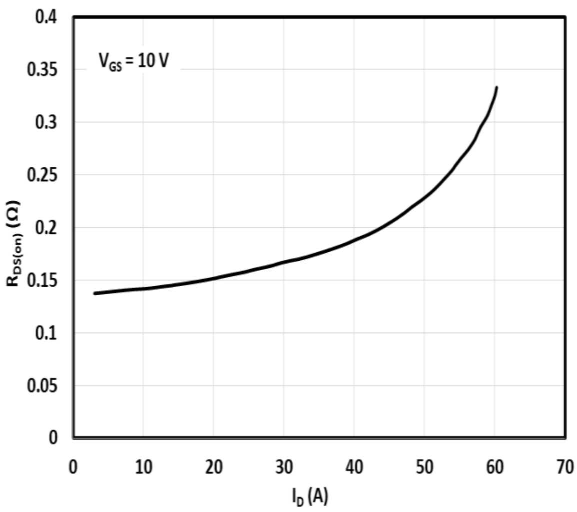


Fig. 6 Typical drain-source on-state resistance

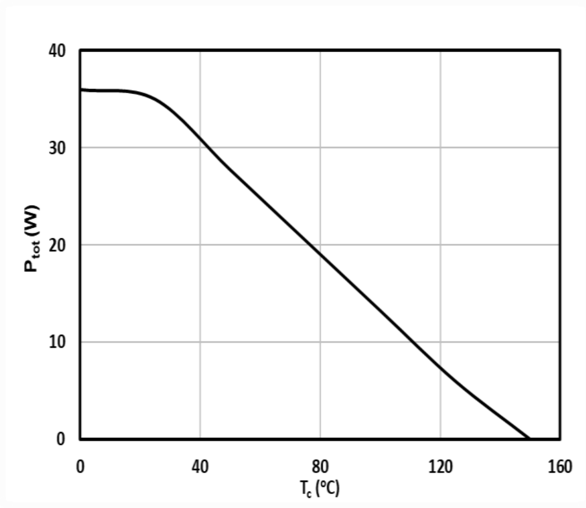


Fig. 7 Typical power dissipation

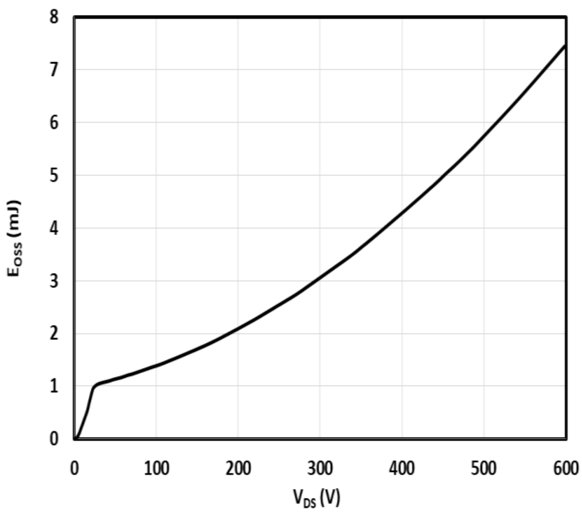


Fig. 8 Typical C_{oss} stored energy

Test Circuits and Waveforms

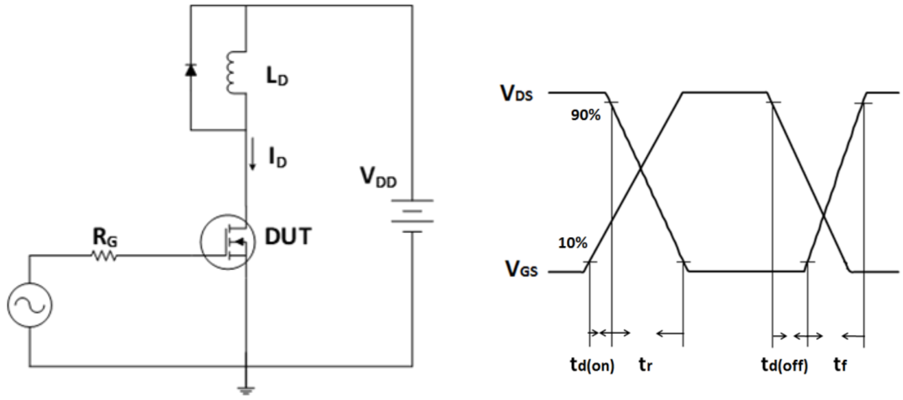


Fig. 1 Inductive switching time test circuit & waveforms

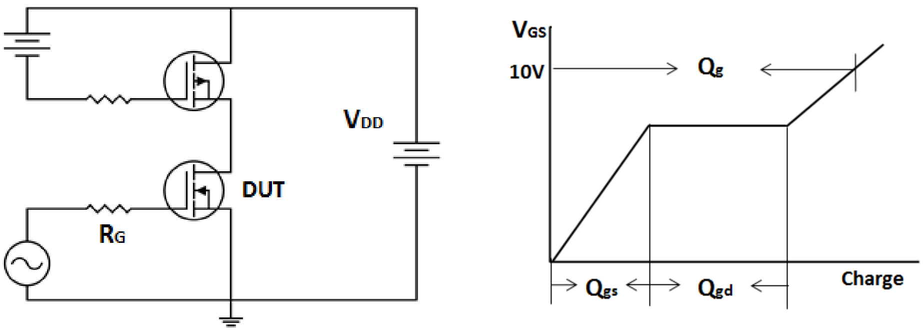


Fig. 2 Gate charge test circuit & waveform

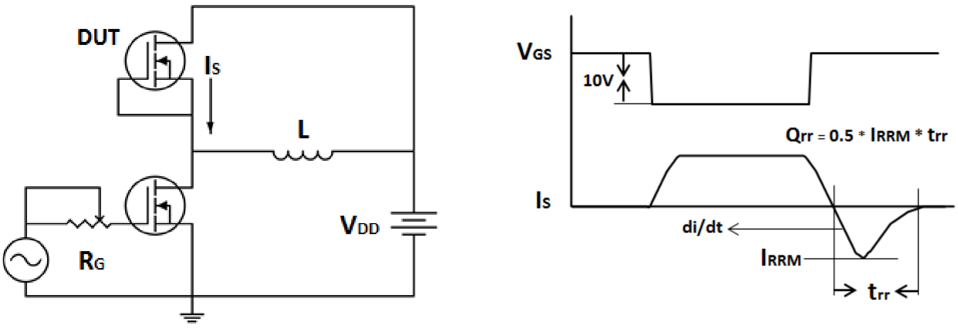


Fig. 3 Peak diode recovery dv/dt test circuit & waveforms

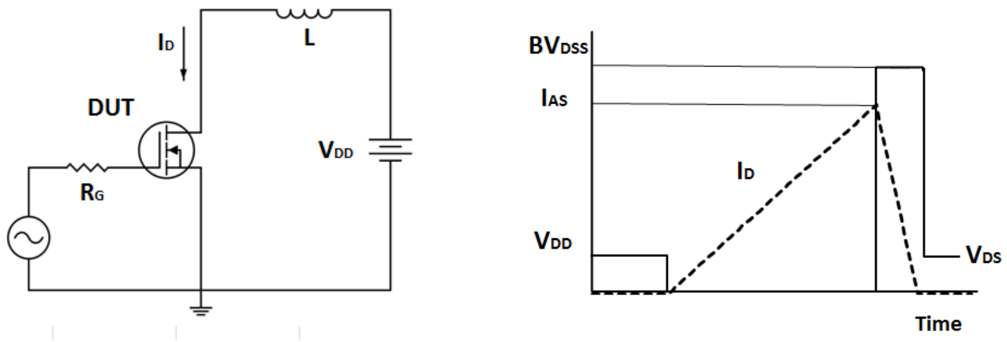
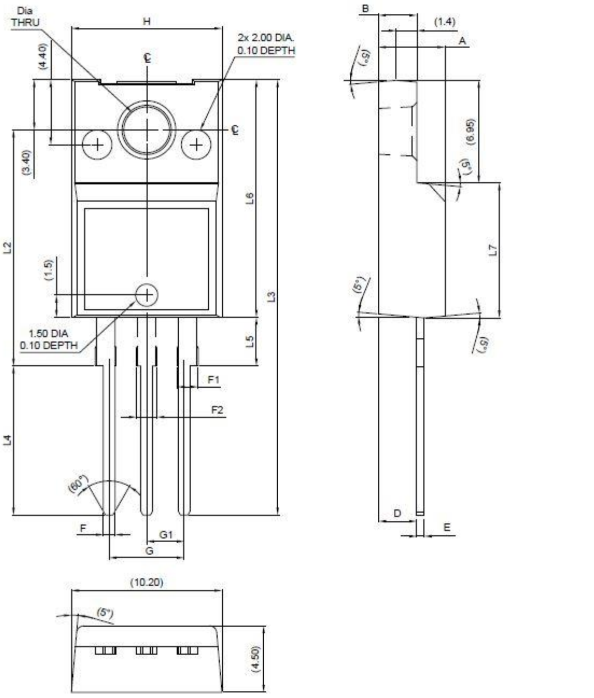


Fig. 4 Unclamped inductive switching test circuit & waveforms

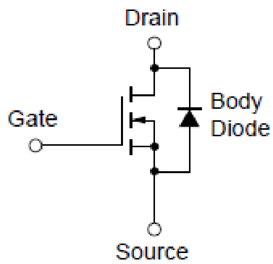
Package Drawing



DIM	MIN	NOM	MAX
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.5
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

TO-220F

Equivalent Circuit



Revision history of JCF60R180S specification

Version	Change Items	Effective Date
0.00	Proposal release.	

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